

1 INTEGRATED CIRCUIT PACKAGING FOR IMPROVING EFFECTIVE 2 CHIP-BONDING AREA

3 4 FIELD OF THE INVENTION

5 The present invention is relating to a process for making an integrated circuit
6 package, particularly to a process for making an integrated circuit package for improving
7 effective chip-bonding area using a B-stage film layer as a chip bond material.

8 BACKGROUND OF THE INVENTION

9 It is conventional technique to utilize B-stage compound to be a chip bond material,
10 as disclosed in R.O.C. Taiwan Patent No. 455,970 entitled "multi-chip stacked package".
11 The conventional B-stage compound is used for adhering two chips, it won't produce a
12 stress between the two chips because the two chips have a same thermal coefficient.
13 Also the B-stage compound is sealed inside the molding compound, so that the adhesive
14 strength of the B-stage compound is not demanded severely.

15 When a B-stage compound is directly configured to adhere a chip to a substrate in
16 integrated circuit package. As showed in Fig.1, at first a B-stage compound 13 is
17 applied to the chip-attaching surface 11 of the substrate 10. Next, the back surface 23 of
18 the chip 20 is compressed to the chip-attaching surface 11 of the substrate 10. The
19 B-stage compound 13 is heated while compressed to become a fully cured C-stage film
20 layer 13 that adheres the chip 20 to the substrate 10 during the chip-attaching step. The
21 C-stage film layer 13 will not have any change in physical phase and any chemical
22 reaction in the sequent process especially the molding step. Bonding wires 30 that are
23 formed by wire-bonding technique connect the bonding pads 21 on the active surface 22
24 of the chip 20 with the pads 12 of the substrate 10, next a molding step is executed.
25 However, the B-stage compound 13 is formed by printing or other liquid dispensing
26 method so as not to have an attaching surface that is not flat completely, and cannot
27 substantially adhere the chip 20 and the substrate 10 by the chip 20 attaching pressure.

1 A popcorn defect is easy to happen while executing reliability test such as moisture or
2 burn-in test after packaging. Therefore, when the chip 20 is separated from the substrate
3 10 prior to molding in a test, it is evident that the C-stage film layer 13 on the substrate
4 10 has a bad effective chip-bonding area merely 50 % approximately against the entire
5 chip-bonding region of the substrate 10, even smaller than 30 % (as showed in Fig.2).
6 For that reason, the C-stage film layer 13 formed in chip-attaching step of the
7 conventional process is not good enough to adhere the chip 20 and the substrate 10, also
8 there are voids or gaps between the chip 20 and the substrate 10.

9 SUMMARY

10 The primary object of this invention is to provide a process for integrated circuit
11 package for improving effective chip-bonding area. Passing through a chip-attaching
12 step and an electrically connecting step, a chip bond material on a substrate is maintained
13 as a B-stage film layer to bond a chip. Next a molding compound is formed on the
14 substrate. Because the packing pressure for the molding compound is larger than the
15 chip-attaching pressure, the B-stage film layer can further closely re-bond the chip for
16 improving effective chip-bonding area in molding step.

17 The secondary object of this invention is to provide a packaging process using a
18 B-stage film layer as a chip bond material. The B-stage film layer closely bonds the
19 chip and the substrate. Because the B-stage film layer has a glass transition temperature
20 (T_g) lower than chip-attaching temperature and has a thermosetting temperature lower
21 than thermosetting temperature of the molding compound, the B-stage film layer can be
22 closely compressed between the chip and the substrate to remove gaps or voids in the
23 molding step.

24 In accordance with this invention, a packaging process for improving effective
25 chip-bonding area comprises a plurality of steps as follows. The first step is to provide
26 a substrate having a chip-attaching surface. Next, an A-stage liquid paste including
27 thermosetting material and solvent is applied to the chip-attaching surface of the substrate.

1 Following, the substrate is heated in order to remove the solvent of the A-stage liquid
2 paste, resulting that the A-stage liquid paste is transformed into a dry B-stage film layer
3 without fully curing. A chip is attached to the chip-attaching surface of the substrate by
4 adhesion of the B-stage film layer, but the B-stage film layer is not cured fully during the
5 chip-attaching step. Then, the chip is electrically connected with the substrate having
6 the B-stage film layer in the next step. Finally, a molding compound is formed by a
7 molding step. The B-stage film layer is active during the molding step. The packing
8 pressure for the molding compound is 1000psi~1500psi approximately that is larger than
9 the chip-attaching pressure, so that the B-stage film layer can be closely compressed to
10 re-bond the chip in order to improve the effective chip-bonding area. Preferably, the
11 heating temperature in the molding step is 150°C~200°C approximately higher than the
12 fully curing temperature of the B-stage film layer so as to cure the B-stage film layer and
13 the molding compound simultaneously.

14 DESCRIPTION OF THE DRAWINGS

15 Fig.1 is a cross sectional view of a substrate with an attached chip in a conventional
16 integrated circuit packaging process.

17 Fig.2 is a photograph showing the effective chip-bonding area on the substrate in the
18 conventional integrated circuit package.

19 Fig.3 is a flow chart of a packaging process for improving effective chip-bonding
20 area in accordance with an embodiment of the present invention.

21 From Fig.4A to Fig.4F are cross sectional views of the substrate in the packaging
22 process in accordance with the embodiment of the present invention.

23 Fig.5 is a cross sectional view of the integrated circuit package formed by the
24 packaging process in accordance with the embodiment of the present invention.

25 Fig.6 is a cross sectional view of a substrate with an attached chip inside a mold in
26 accordance with another embodiment of the present invention.

27 DETAILED DESCRIPTION OF THE PRESENT INVENTION

1 Referring to the drawings attached, the present invention will be described by means
2 of the embodiments below.

3 According to an embodiment of the present invention, the packaging process for
4 improving effective chip-bonding area comprises the steps as showed in Fig.3.

5 As showed in Fig.3 and Fig.4A, the first step 101 is to provide a substrate 110, the
6 substrate 110 is a high density wiring substrate for integrated circuit package, such as BT
7 printed circuit board, thin film wiring board or TAB tape. The substrate 110 has a
8 chip-attaching surface 111, and a plurality of connect pads 112 (or fingers) are formed on
9 the chip-attaching surface 111 for electrically connecting with the chip 130. But the
10 location of the connect pads 112 is not limited, the connect pads 112 can be formed on
11 the other surface of the substrate 110 in another instance. Advantageously, the other
12 surface of the substrate 110 corresponding to the chip-attaching surface 111 is a
13 surface-mounting surface 113 that is electrically connected with the chip-attaching
14 surface 111 by vias.

15 Next, as showed in Fig.3 and Fig.4B, an applying step 102 is executed. An A-stage
16 liquid paste 121 is formed on the chip-attaching surface 111 of the substrate 110 to be
17 used as a chip bond material. The A-stage liquid paste 121 may be formed by a liquid
18 coating method, such as printing, screen printing, stencil printing, spraying, spin coating
19 or dipping method. In this embodiment, the A-stage liquid paste 121 is formed by
20 screen printing technique without covering the connect pads 112. The A-stage liquid
21 paste 121 includes multi-stage thermosetting resins such as polyimide, polyquinolin or
22 benzocyclobutene and a solvent that may dissolve the foregoing thermosetting resins
23 such as the mixed solvent of butyrolactone and cyclopentanone or 1,3,5-mesitylene.
24 The glass transition temperature (T_g) of the A-stage liquid paste 121 should be between
25 -40°C and 10°C.

26 Next, as showed in Fig.3 and Fig.4C, the heating step 103 is followed. The
27 substrate 110 is heated to pre-curing the A-stage liquid paste 121. The solvent of the

1 A-stage liquid paste 121 is removed by heating, vacuum drying or ultraviolet rays curing
2 so that the A-stage liquid paste 121 is transformed into a dry and adhesive B-stage film
3 layer 122. The B-stage film layer 122 is thermoplastic and thermosetting property and
4 generally is called "prepreg". The B-stage film layer 122 has a glass transition
5 temperature (T_g) and a fully curing temperature. The B-stage film layer 122 is active to
6 present various adhesive under various temperatures. The glass transition temperature
7 (T_g) of the B-stage film layer 122 is between $-10^{\circ}\text{C}\sim 100^{\circ}\text{C}$ approximately, preferably
8 between $35^{\circ}\text{C}\sim 70^{\circ}\text{C}$. When the B-stage film layer 122 is under a temperature higher
9 than the glass transition temperature (T_g) of the B-stage film layer 122 but lower than the
10 fully curing temperature, the B-stage film layer 122 will becomes viscous and adhesive
11 for attaching a chip. When the B-stage film layer 122 on the substrate 110 is under a
12 temperature (about $<35^{\circ}\text{C}$) lower than the glass transition temperature of the B-stage
13 film layer 122, such as room temperature, the B-stage film layer 122 will become a dry
14 film without adhesive for transporting and storing the substrate 110. Also, the fully
15 cured temperature of the B-stage film layer 122 is about 175°C close to the molding
16 temperature in the molding step 106.

17 Then, as showed in Fig.3 and Fig.4D, the chip attaching step 104 is executed. A
18 chip 130 is attached to the chip-attaching surface 111 of the substrate 110 under a raised
19 temperature and a pressure, wherein the temperature for attaching the chip 130 should be
20 higher than the glass transition temperature of the B-stage film layer 122. The B-stage
21 film layer 122 becomes adhesive to bond the chip 130 with the substrate 110. In this
22 embodiment, the back surface 133 of the chip 130 is bonded on the chip-attaching surface
23 111 of the substrate 110 by the B-stage film layer 122 according to correspondingly
24 various packages. There are a plurality of the bonding pads 131 formed on the active
25 surface 132 of the chip 130. It is important that the B-stage film layer 122 is maintained
26 in a partially curing condition without fully curing the B-stage film layer 122 during the
27 chip attaching step 104 and the electrically connecting step 105.

1 Thereafter, as showed in Fig.3 and Fig.4E, the electrically connecting step 105 is
2 executed. The bonding pads 131 of the chip 130 are electrically connected with the
3 connect pads 112 of the substrate 110 by the metal wires 140 that are formed by wire
4 bonding. At this time, the B-stage film layer 122 is maintained without fully curing.
5 Besides, tape automated bonding method (TAB) or other conventional techniques can be
6 utilized for this electrical connection.

7 Finally, as showed in Fig.3 and Fig.4F, the molding step 106 is performed. The
8 molding step 106 includes a filling sub-step and a packing sub-step for forming a
9 molding compound 150 on the substrate 110 by molds 151,152. In the filling sub-step,
10 the substrate 110 with the attached chip 130 and the B-stage film layer 122 is placed
11 inside the mold cavity formed by an upper mold 151 and a lower mold 152. A molding
12 compound 150 is filled into the mold cavity under a filling pressure until filling over 80
13 vol% of the mold cavity. The molding compound 150 includes thermosetting resin,
14 curing agent, silicate filler, releasing wax and a few coloring agent. In the packing
15 sub-step, the packing pressure higher than the filling pressure is applied to the molding
16 compound 150 inside the mold cavity to remove voids in the molding compound 150 and
17 the voids in the B-stage film layer 122. The packing pressure is about 1000psi ~1500psi
18 approximately larger than the chip attaching pressure mentioned in the chip attaching step
19 104. After completing the chip attaching step 104 and the electrically connecting step
20 105, the B-stage film layer 122 is still in partially curing condition and can be deformed
21 suitably. The B-stage film layer 122 is closely compressed under the high packing
22 pressure for the molding compound 150, so that the voids and gaps inside the B-stage
23 film layer 122 will be removed so as to improve effective chip-bonding area between the
24 chip 130 and the substrate 110. Preferably, the heating temperature in the molding step
25 106 for curing the molding compound 150 is about 150°C~200°C that matches the fully
26 curing temperature of the molding compound 150, so that the B-stage film layer 122 and
27 the molding compound 150 are cured simultaneously. After the molding step 106, the

1 B-stage film layer 122 is transformed into the C-stage film layer 123 (as showed in Fig.5)
2 to be a stable fixed film layer. In this embodiment, a step follows the molding step 106
3 to plant a plurality of solder balls 160 on the surface-mounting surface 113 of the
4 substrate 110, then the substrate 110 is diced and separated to construct a ball grid array
5 (BGA) package with excellent reliability. The packaging process for improving
6 effective chip-bonding area of the present invention is suitable for various packages,
7 especially for chip scale package (CSP). The B-stage film layer 122 won't contaminate
8 the connect pads 112 of the substrate 110, so that the connect pads 112 may be arranged
9 to be closely near to the chip 130. Advantageously, after dicing the substrate 110 to
10 form separate integrated circuit package, the chip-attaching surface 111 of the substrate
11 110 is not larger than 1.5 times the active surface 132 of the chip 130 in area so as to
12 form a chip scale package (CSP).

13 Furthermore, the packaging process for improving effective chip-bonding area of the
14 present invention can be utilized for other different packages. As showed in Fig.6, a
15 substrate 210 has a window 214, a B-stage film layer 222 is printed on a chip-attaching
16 surface 211 of the substrate 210 for bonding the active surface 232 of the chip 230. The
17 B-stage film layer 222 has a coating region larger than the active surface 232 of the chip
18 230. Bonding pads 231 are formed on the active surface 232 of the chip 230, the active
19 surface 232 of the chip 230 is attached to the chip-attaching surface 211 of the substrate
20 210 corresponding to the window 214 to expose from the bonding pads 231. The
21 bonding pads 231 of the chip 230 are electrically connected with the connect pads 212 of
22 the substrate 210 by the bonding wires 240. The B-stage film layer 222 is not fully
23 cured during the chip attaching step 104 and the electrically connecting step 105. When
24 the substrate 210 is sealed by an upper mold 251 and a lower mold 252, the packing
25 pressure for the molding compound 250 also make the B-stage film layer 222 be closely
26 compressed in order to improve effective chip-bonding area.

27 The above description of embodiments of this invention is intended to be illustrated

1 are not limiting. Other embodiments of this invention will be obvious to those skilled in
2 the art in view of the above disclosure.

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